CLAIMS

1. A method for compensating for temperature effects during operation of a semiconductor circuit comprising:

scaling an output value of said circuit to a desired output value at a first temperature; and

matching said output value, at a second temperature, to said desired output value, whereby said desired output value at said first temperature remains unchanged.

2. The method of claim 1 wherein the step of scaling said output value is effected by the addition or subtraction of a constant voltage value.

3. The method of claim 2 wherein said constant voltage value is generated by forcing a constant current through a resistor of said circuit.

4. The method of claim 3 comprising generating said current from a balanced combined PTAT and CTAT current.

5. The method of claim 3 comprising generating said current from reflecting a reference voltage across said resistor.

6. The method of claim 1 wherein the matching step is effected by the addition or subtraction of the difference between two balanced trimming PTAT and CTAT currents.

7. The method of claim 6 wherein said trimming currents are such that at said first temperature the difference between each current is zero and the combined current value has a double slope compared to a slope value of each individual current.

8. The method of claim 6, between said scaling and said matching step, comprising the additional step of tuning of said trimming currents such that the difference between said PTAT and CTAT currents at said first temperature is equal to zero.

9. The method of claim 1 wherein the step of scaling comprises scaling a straight line defined by two points to fit a straight line intersecting a fixed determined point at said first temperature.

10. The method of claim 9 wherein the step of matching comprises rotating said straight line about said fixed determined point at said second temperature.

11. A method for compensating for temperature effects during operation of a semiconductor circuit comprising:

scaling an output voltage of said circuit to a desired output voltage value at a first temperature by a temperature independent voltage; and

correcting at a second temperature the slope of a line representative of said desired output voltage over a temperature range to provide said desired output voltage at said second temperature by adding or subtracting a correcting voltage whereby said correcting voltage is always zero at said first temperature, and whereby said desired output voltage value at said first temperature remains unchanged.

12. The method according to claim 11 wherein the step of scaling the output voltage is effected by an addition or subtraction of the output voltage by a constant voltage value.

13. The method of claim 11 where the slope of the line is defined by two points, the first point being the desired output voltage value at said first temperature, and the second point being the value of the output voltage at said second temperature.

14. The method of claim 11 wherein the correcting voltage is the value of the difference between two balanced trimming PTAT and CTAT currents reflected across a resistor of said circuit.

15. The method of claim 14 wherein said trimming currents are such that at said first temperature the difference between each current is zero and the combined current value has a double slope compared to the slope of each individual current.

16. The method of claim 14, between said scaling and correcting step, comprising an additional step of tuning said trimming currents such that the difference between said PTAT and CTAT currents at said first temperature is equal to zero.

17. A semiconductor circuit adapted to provide compensation for temperature effects during operation comprising:

means for scaling an output of said circuit to a desired output value at a first temperature; and

means for matching said output value, at a second temperature, to said desired output value, whereby said desired output value at said first temperature remains unchanged.

18. The circuit of claim 17 wherein the means for scaling said output comprises a multiplexor for adding or subtracting said output by a constant voltage value.

19. The circuit of claim 18 wherein the constant voltage value is generated by forcing a constant current through a resistor of said circuit.

20. The circuit of claim 19 wherein the value of the constant current is controlled by a current source coupled to a DAC, a value of a user controlled input code applied to said DAC to determine the value of the constant current.

21. The circuit of claim 20 wherein the addition or subtraction of the constant voltage value is controlled by at least one of said multiplexors coupled to two outputs of said DAC, to determine whether the constant voltage value is to be added or subtracted.

22. The circuit of claim 20 wherein the addition or subtraction of the constant voltage value is controlled by a second input to the said DAC.

23. The circuit of claim 17 wherein the means for matching is provided by the addition or subtraction of the difference between two balanced trimming PTAT and CTAT currents.

24. The circuit of claim 23 wherein said trimming currents are such that at said first temperature the difference between each current is zero and the combined current value has a double slope in the temperature domain compared to the slope of each individual trimming current.

25. The circuit of claim 23 wherein the PTAT and CTAT trimming currents are controlled by a first and a second DAC, the output of said first and second DAC connected to at least one multiplexor, whereby a control signal applied to said multiplexor controls the addition or subtraction of said difference.

26. The circuit of claim 23 comprising tuning means for the tuning of said trimming currents such that the difference between said PTAT and CTAT currents at said first temperature is equal to zero.

27. The circuit of claim 26 wherein said tuning means is provided by means of a tuning DAC coupled to one of said currents, by adjusting a value of a user controlled input to said tuning DAC.

28. The circuit of claim 20 wherein the values of the user controlled inputs codes are stored in memory.

29. The circuit of claim 27 wherein the value of the user controlled input code is stored in memory.

30. The circuit of claim 24 wherein the value of said trimming currents providing said difference are stored in memory.

31. A semiconductor circuit adapted to provide compensation for temperature effects during operation, the circuit comprising a digital control means for:

digitally scaling an output voltage of said circuit to a desired output voltage value at a first temperature; and

digitally matching said output voltage value, at a second temperature, to said desired output voltage value, whereby said desired output voltage value at said first temperature remains unchanged.

32. The semiconductor circuit of claim 31 wherein a constant current is generated by a balanced combination of PTAT and CTAT current sources, each current source coupled to a DAC, the value of an input code applied to an input of each DAC determining the value of the constant current, and wherein the addition or subtraction of the constant voltage value is controlled by a second input to each DAC.

33. The semiconductor circuit of claim 31 wherein said digital control means comprises a register, coupled to the inputs of each DAC, wherein the output values from said register determine the value of the input codes to each DAC.

34. The semiconductor circuit of claim 33 wherein said register is connected to a digital control unit and memory, the value of said input codes are stored in said memory, and the transfer of said input codes from memory to the register is controlled by said digital control unit.

35. A computer program product comprising a medium having embodied therein program instructions for causing a computer to perform the method of claim 1, when executed.

36. A computer program product comprising a medium having embodied therein program instructions for causing a computer to perform the method of claim 1 when executed, wherein the medium includes a carrier signal.

37. A computer program product comprising a medium having embodied therein program instructions for causing a computer to perform the method of claim 1 when executed, wherein the medium includes a read-only memory.